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2215A OSCILLOSCOPE

SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-4735-00
Product Group 46

Serial Number _____

First Printing DEC 1983
Revised JUL 1984

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The Alternate B Sweep circuitry controls the Alt and B Horizontal mode displays and includes the B Miller Sweep Generator and B Sweep Logic circuitry. In addition to providing the B Sweep sawtooth waveform, signals are generated which control the display switching between the A and B displays.

The intensity levels of both the A and B Sweeps are set by the front-panel A and B INTENSITY controls. These controls, along with signals from the A and B Sweep Logic circuits, determine the drive level to the Z-Axis Amplifier.

The Z-Axis drive from both the A Sweep Logic circuit and the Alternate B Sweep circuit is applied to the Z-Axis Amplifier. The output signal from the Z-Axis Amplifier circuit sets the crt intensity. When using Chop Vertical mode, a blanking signal from the Chop Oscillator circuit blanks the crt display while switching between the vertical channels.

The Dc Restorer circuit applies the output voltage of the Z-Axis Amplifier between the cathode and grid of the crt. High dc potentials on these elements prohibit direct coupling to the crt.

The Power Supply provides the necessary operating voltages for the instrument. Operating potentials are obtained from a circuit composed of the Preregulator, Inverter and Transformer, and Rectifiers and Filters. The Preregulator produces approximately +43 V dc from the ac power line which is used to drive the 20 kHz Inverter stage. The transformer secondary windings provide various ac levels that are rectified and filtered to produce the operating voltages. A high-voltage multiplier circuit produces the accelerating, focus, and cathode potentials required by the crt.

A front-panel PROBE ADJUST output is provided for use in adjusting probe compensation. The voltage at the PROBE ADJUST connector is a negative-going square wave that has a peak-to-peak amplitude of approximately 0.5 V and a repetition rate of approximately 1 kHz.

DETAILED CIRCUIT DESCRIPTION

VERTICAL ATTENUATORS

The Channel 1 and Channel 2 Attenuator circuits, shown on Diagram 1, are identical with the exception of the additional Invert circuitry in the Channel 2 Paraphase Amplifier. Therefore, only the Channel 1 Attenuator will be described and the Invert circuitry of Channel 2 will be discussed separately.

The Attenuator circuit (see Figure 3-1) provides control of input coupling, vertical deflection factor, and variable volts-per-division gain. Input signals for crt vertical deflection may be connected to the CH 1 OR X and the CH 2 OR Y input connectors. In the X-Y mode of operation, the signal applied to the CH 1 OR X connector provides horizontal (X-Axis) deflection for the display, and the signal applied to the CH 2 OR Y connector provides the vertical (Y-Axis) deflection for the display.

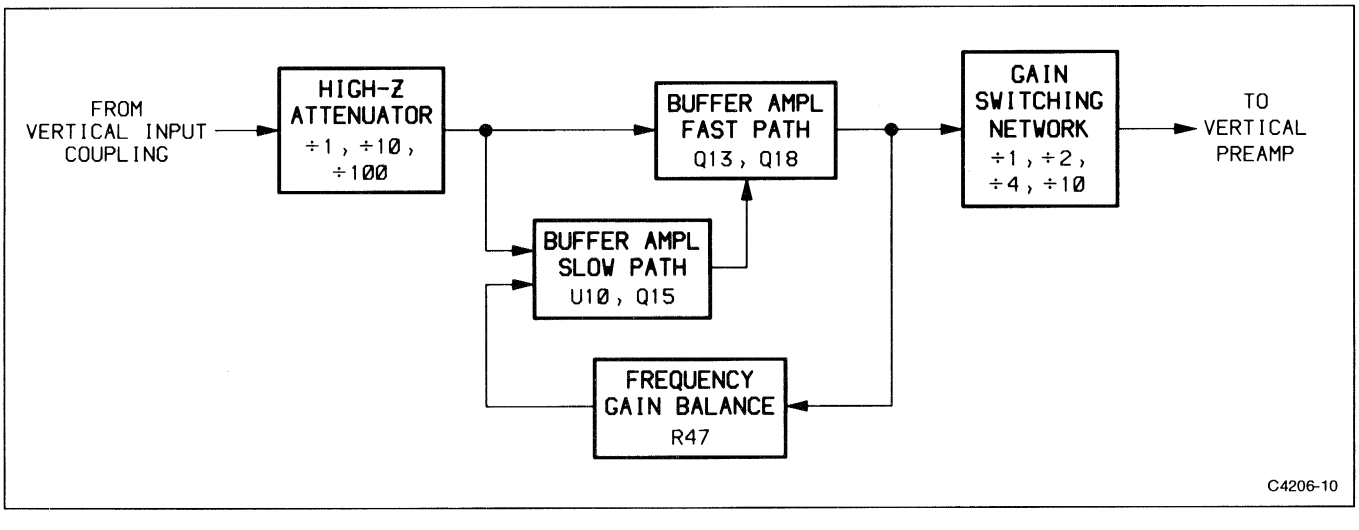


Figure 3-1. Block diagram of the Vertical Attenuators.

Input Coupling

The signal applied to the CH 1 OR X input connector can be ac coupled, dc coupled, or disconnected from the input of the High-Impedance Input Attenuator circuit. Signals applied to the CH 1 OR X input connector are routed through resistor R9100 to Input Coupling switch S1. When S1 is set for dc coupling, the Channel 1 signal is applied directly to the input of the High-Impedance Attenuator stage. When ac coupled, the input signal passes through dc-blocking capacitor C2. The blocking capacitor prevents the dc component of the input signal from being applied to the Attenuator circuit. When switched into the signal path, attenuators AT1 and AT2 attenuate the input signal by factors of 100 and 10 respectively. When S1 is set to GND, the direct signal path is opened and the input of the Buffer Amplifier is connected to ground. This provides a ground reference without the need to disconnect the applied signal from the input connector. The coupling capacitor precharges through R4 to prevent large trace shifts when switching from GND to AC.

Buffer Amplifier and Gain Switching Network

The Buffer Amplifier presents a high-impedance, low-capacitance load to the signal from the High-Impedance Attenuator and a low output impedance to the Gain Switching Network. A dual-path amplifier is used to combine high-dc stability with high-speed performance.

In the slow path, the input signal is applied to both the gate of source-follower Q13 and the inverting input of U10 through the divide-by-two network composed of R3 and R5. Transistor Q13 and emitter-follower Q18 isolate the input signal from the loading of the Gain Switching Network. The divider network at the output of the Amplifier (R46, R47, and R48) is connected to the other input of U10. Amplifier U10 compares the two divider voltages and changes the conduction level of current-source transistor Q15 to correct for any error at the source of Q13. Capacitor C10 limits the bandwidth of U10 so that the slow path responds only to frequencies below 100 kHz.

In the fast path, input signals are coupled through R6, C6, Q13, and Q18 to the circuit output. By adjusting R47, the gain in both paths is matched. Input offset voltage compensation for U10 is provided by R10 to eliminate trace shifts when switching between Volts/Div settings.

The Gain Switching Network divides down the Buffer Amplifier output signal for application to the Paraphase Amplifier and has an output impedance of 75 Ω for all Volts/Div switch settings. The particular Volts/Div switch setting will determine which contacts of S10 are closed and therefore whether the Paraphase Amplifier will receive a ÷ 1, ÷ 2, ÷ 4, or ÷ 10 signal.

Paraphase Amplifier

The Paraphase Amplifier converts the single-ended signal from the Gain Switching Network into a differential signal for application to the Vertical Preamplifier. Included in the circuitry is switching that provides extra gain for the 2 mV position of the VOLTS/DIV switch, adjustments for amplifier dc balance, and circuitry for the Variable Volts/Div function. Additionally, the Channel 2 Paraphase Amplifier contains circuitry to invert the Channel 2 display.

The signal from the Gain Switching Network is applied to the base of one transistor in U30. The other input transistor is biased by the divider network composed of R30, R31, and R33 to a level that will produce a null between the outputs of U30 (no trace shift on the crt screen) when the VOLTS/DIV control is switched between 5 mV and 2 mV. Emitter current for the two input transistors is supplied by R21, R22, R23, and R25, with R29 serving as the gain-setting resistor between the two emitters. In the 2 mV position, amplifier gain is increased by closing contact 15 of S10 to shunt R29 with R26.

The collector current through the two input transistors serves as emitter current for the two differential output transistor pairs. Base-bias voltages for the two pairs are derived from the divider network composed of R39, R41, R42, and R43. Monolithic IC U30 has matched transistor characteristics, so the ratio of currents in the two diodes connected to pin 11 determines the current ratios in the output transistor pairs. As VOLTS/DIV Variable potentiometer R43 is rotated from the calibrated to uncalibrated position, the conduction level of the transistors connected to R35 will increase. Since the transistor pair outputs are cross-wired, this increased conduction will subtract from the signal produced by the transistors connected to R38 and the overall gain of the Amplifier will decrease. Potentiometer R25 adjusts the balance of the Amplifier so there is minimal dc trace shift as the VOLTS/DIV Variable control is rotated.

Incorporated in the Channel 2 Paraphase Amplifier is circuitry to invert the polarity of the Channel 2 signal. When INVERT switch S90 is out, the transistor pairs in U80 are biased as they are in U30 and there is no trace inversion. For the IN position of S90, connections to the bases of the output transistor pairs are reversed to produce an inverted Channel 2 trace. Potentiometer R75 is adjusted so that there is minimal dc trace shift as the INVERT button is changed between the IN and OUT positions.

VERTICAL PREAMPLIFIERS

The Vertical Preamplifier, shown on Diagram 2, utilizes differential signal current from the Paraphase Amplifier to

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				ASSEMBLIES		
A1	670-8284-00	B010100	B011899	CKT BOARD ASSY:MAIN	80009	670-8284-00
A1	670-8284-01	B011900		CKT BOARD ASSY:MAIN	80009	670-8284-01
A2	672-0086-00			CKT BOARD ASSY:ATTENUATOR	80009	672-0086-00
A2A1	670-8267-XX			CKT BOARD ASSY:ATTENUATOR		
	----- -----			(NOT REPLACEABLE,USE A2)		
A3	670-8286-00			CKT BOARD ASSY:FRONT PANEL	80009	670-8286-00
A4	670-8285-00			CKT BOARD ASSY:TIMING	80009	670-8285-00
A5	670-8287-00			CKT BOARD ASSY:ALTERNATE SWEEP	80009	670-8287-00
A6	670-7615-00			CKT BOARD ASSY:EMI FILTER BOARD	80009	670-7615-00
				A1 MAIN		
A1	670-8284-00	B010100	B011899	CKT BOARD ASSY:MAIN	80009	670-8284-00
	670-8284-01	B011900		CKT BOARD ASSY:MAIN	80009	670-8284-01
A1C114	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A1C115	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A1C116	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C125	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A1C126	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	59660	805534Y5DO152J
A1C130	283-0642-00			CAP.,FXD,MICA D:33PF,+/-0.5PF,300V	00853	D10-5E330G
A1C133	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	GC101A680K
A1C164	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A1C165	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A1C175	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A1C176	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	59660	805534Y5DO152J
A1C180	283-0642-00			CAP.,FXD,MICA D:33PF,+/-0.5PF,300V	00853	D10-5E330G
A1C200	290-0136-00			CAP.,FXD,ELCTLT:2.2UF,20%,20V	56289	162D225X0020CD2
A1C201	290-0136-00			CAP.,FXD,ELCTLT:2.2UF,20%,20V	56289	162D225X0020CD2
A1C210	281-0511-00			CAP.,FXD,CER DI:22PF,+/-2.2PF,500V	59660	301-000C0G0220K
A1C215	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C220	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A1C225	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C226	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C228	281-0630-00			CAP.,FXD,CER DI:390PF,5%,500V	72982	630000Y5D391J
A1C229	281-0630-00			CAP.,FXD,CER DI:390PF,5%,500V	72982	630000Y5D391J
A1C237	281-0140-00			CAP.,VAR,CER DI:5-25PF,100V	59660	518-023A 5-25
A1C239	281-0776-00			CAP.,FXD,CER DI:120PF,5%,500V	04222	SA101A121JAA
A1C240	283-0331-00			CAP.,FXD,CER DI:43PF,2%,100V	59660	0805536C0G0-430G
A1C241	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	96733	R3247
A1C242	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C250	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	56289	292CC0G471M100B
A1C251	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	56289	292CC0G471M100B
A1C255	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C262	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M
A1C274	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C281	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C292	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A1C312	281-0895-00			CAP.,FXD,CER DI:6.8PF,100W VDC	04222	MA101A6R8DAA
A1C337	281-0895-00			CAP.,FXD,CER DI:6.8PF,100W VDC	04222	MA101A6R8DAA
A1C363	281-0862-00			CAP.,FXD,CER DI:0.001UF,+80-20%,100V	04222	GC70-1E102M

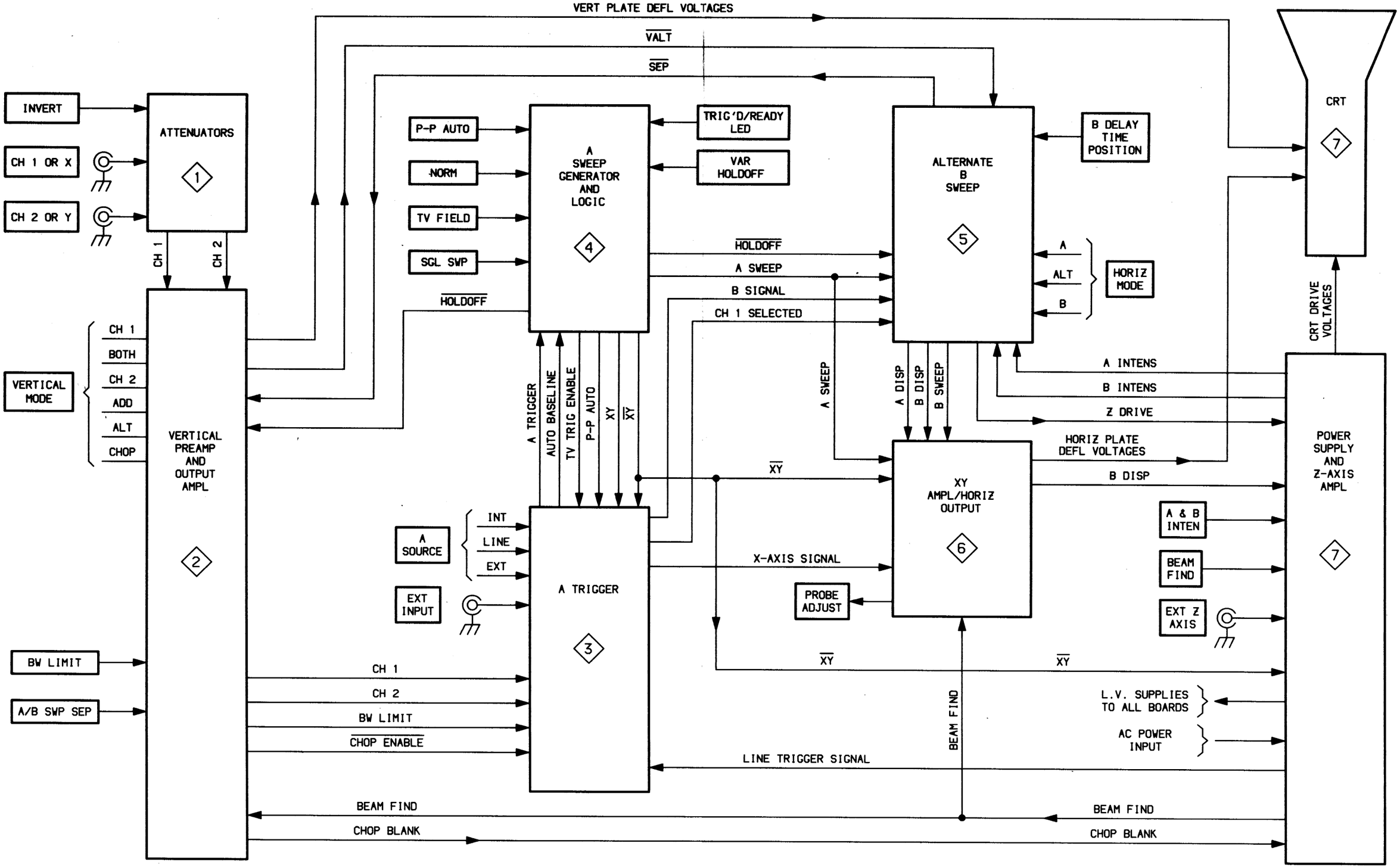


Figure 9-4. Basic block diagram.

CH 1 & CH 2 ATTENUATORS ◇1

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
AT1	2D	3D	C96	9B	4F	R8	2B	3C	R64	6G	7G
AT2	2E	3E	C97	7H	8H	R9	2G	4G	R65	7G	8G
AT51	6D	7D				R10	3G	4F	R67	6H	6H
AT52	6E	7E	CR7	1G	3G	R11	3G	4G	R68	6H	7H
			CR18	2H	3H	R13	1G	3G	R69	6J	7J
C2	2B	3C	CR57	6G	7G	R14	2H	3G	R71	7L	8L
C3	2F	3F	CR68	6H	7H	R15	2G	4G	R72	7L	8L
C4	2D	3D				R17	1H	3H	R73	7L	7L
C5	2D	4D	E90	8B	3F	R18	2H	4H	R75	7L	8L
C6	1G	3F	E91	8B	3F	R19	1J	3J	R76	7M	8L
C9	2G	4G				R21	3L	4L	R79	7N	8M
C10	3G	4F	L93	9B	3F	R22	3M	4L	R80	7M	8M
C11	2E	3E	L96	9B	3F	R23	2M	4L	R81	8N	8M
C12	2E	4E				R25	2M	4L	R83	8M	8L
C13	1H	3G	P9103-1	2S	4S	R26	3M	4L	R84	8N	9M
C17	2H	3H	P9103-2	2S	3S	R29	2N	4M	R85	9N	9N
C21	2L	4L	P9103-3	3S	5S	R30	3M	5M	R87	8N	9N
C30	3M	5M	P9103-4	3S	4S	R31	3N	5M	R88	9P	9N
C35	5N	6N	P9108-1	7S	8S	R33	3M	5L	R91	9M	9M
C38	4P	5P	P9108-2	6S	7S	R34	4N	5M	R93	9M	9M
C52	6B	7C	P9108-3	8S	4E	R35	5N	6N	R96	7H	8H
C53	6F	7F	P9108-4	7S	8S	R37	4P	5N	R97	8H	8H
C54	6D	7D	P9200-1	9L	3A	R38	4P	5N	R98	8H	8H
C55	6D	7D	P9200-2	9L	3A	R39	4P	5P			
C56	6G	4C	P9991-1	8B	8A	R41	4P	5P	S1	4B	5B
C59	7G	8G	P9991-2	9B	9A	R42	5P	6P	S10	4H	5F
C60	7G	8F	P9991-3	9B	9A	R43	5P	6P	S51	5B	6B
C61	6E	7E				R46	3H	4H	S60	5H	6F
C62	6E	7E	Q13	1H	3G	R47	3H	5H			
C63	6H	4C	Q15	2H	4G	R48	3H	5H	U10	2F	4F
C67	6H	7H	Q18	2H	3H	R52	6A	7B	U30	1N	3N
C71	7L	8L	Q63	6H	7G	R53	6F	7F	U60	6F	7F
C76	7M	8M	Q65	7G	8G	R54	6B	7B	U80	6N	7N
C77	7N	8M	Q68	6H	7H	R55	7F	8F			
C80	8M	8M				R56	6G	7F	W43	5P	6P
C85	9N	3E	R2	2A	3B	R57	6D	7D	W93	9M	3F
C88	9P	9N	R3	2F	4F	R58	6B	7C	W94	9C	2F
C90	8B	2F	R4	2B	3B	R59	7G	7G	W96	9C	4F
C91	8B	4F	R5	2F	4F	R60	7G	8F			
C93	9B	2F	R6	2G	3F	R61	7G	8G			
C94	3H	4H	R7	2D	4D	R63	5G	6G			

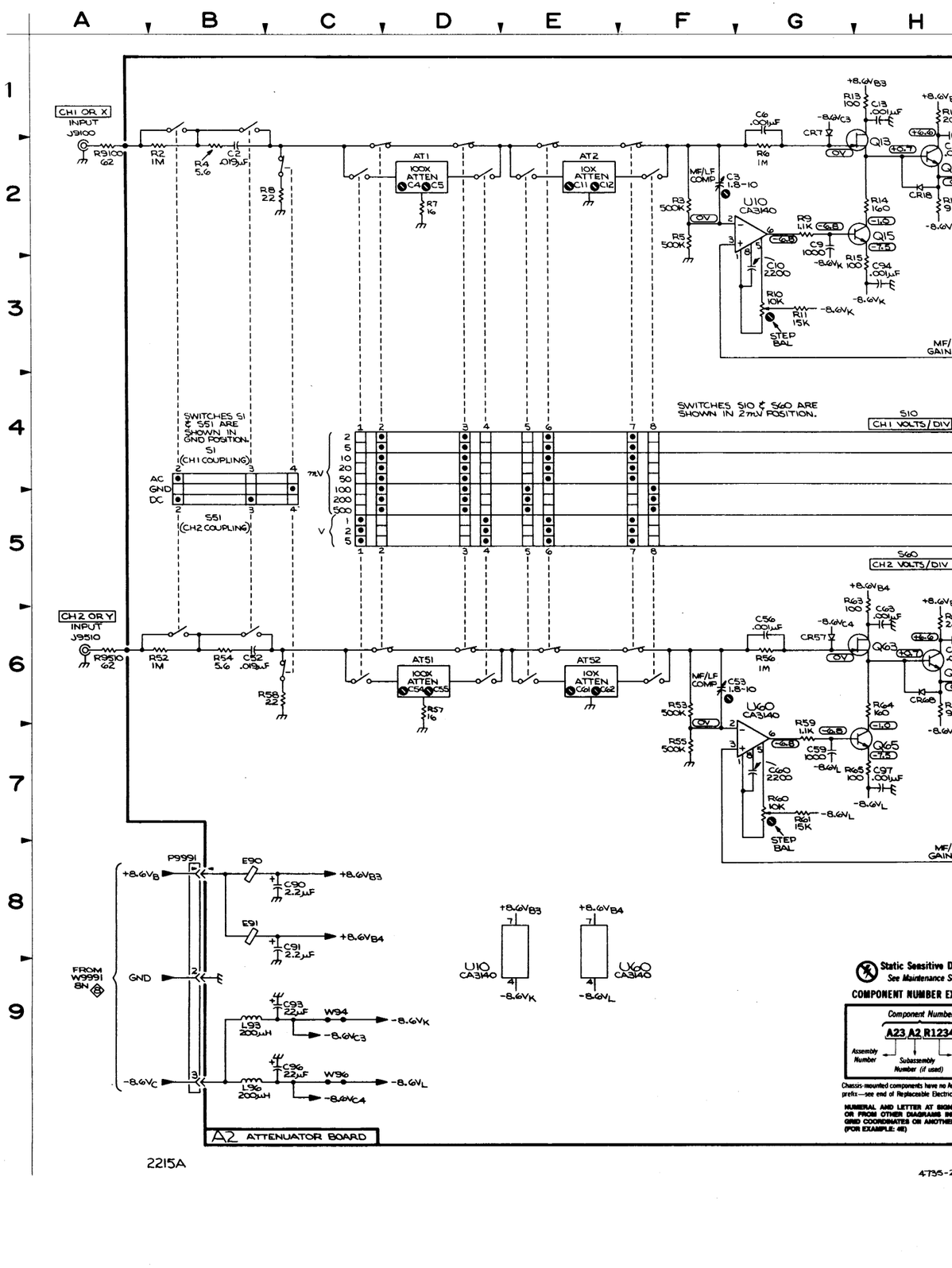
ASSEMBLY A3

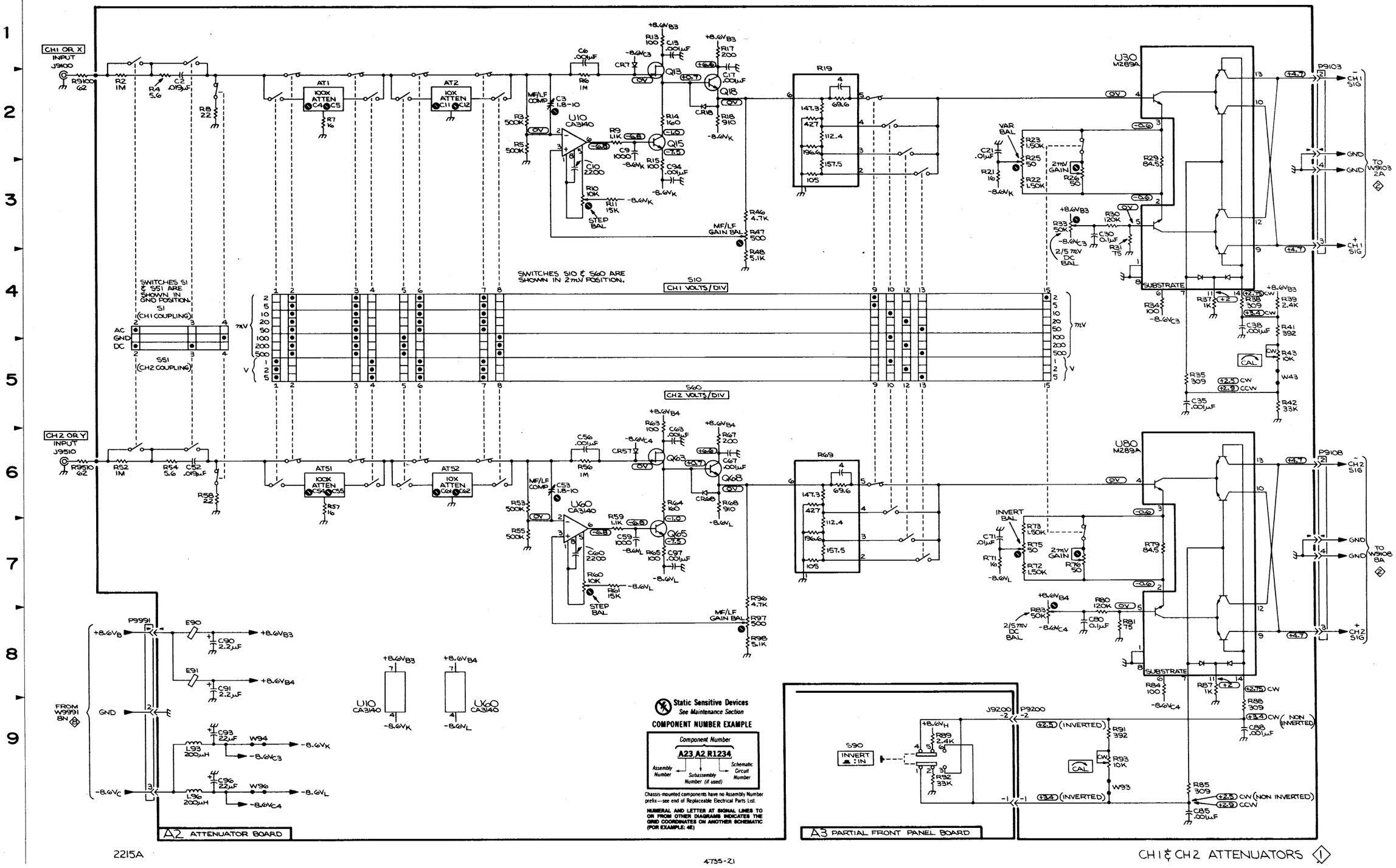
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J9200-1	9L	9K	R89	9K	9K	S90	9K	9J			
J9200-2	9L	9K	R92	9K	9K						

Partial A3 also shown on diagrams 2, 3, 4, 5, 6, 7 and 8.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J9100	1A	CHASSIS	R9100	1A	CHASSIS						
J9510	6A	CHASSIS	R9510	6A	CHASSIS						





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4735-21

CH1 & CH2 ATTENUATORS ◇1

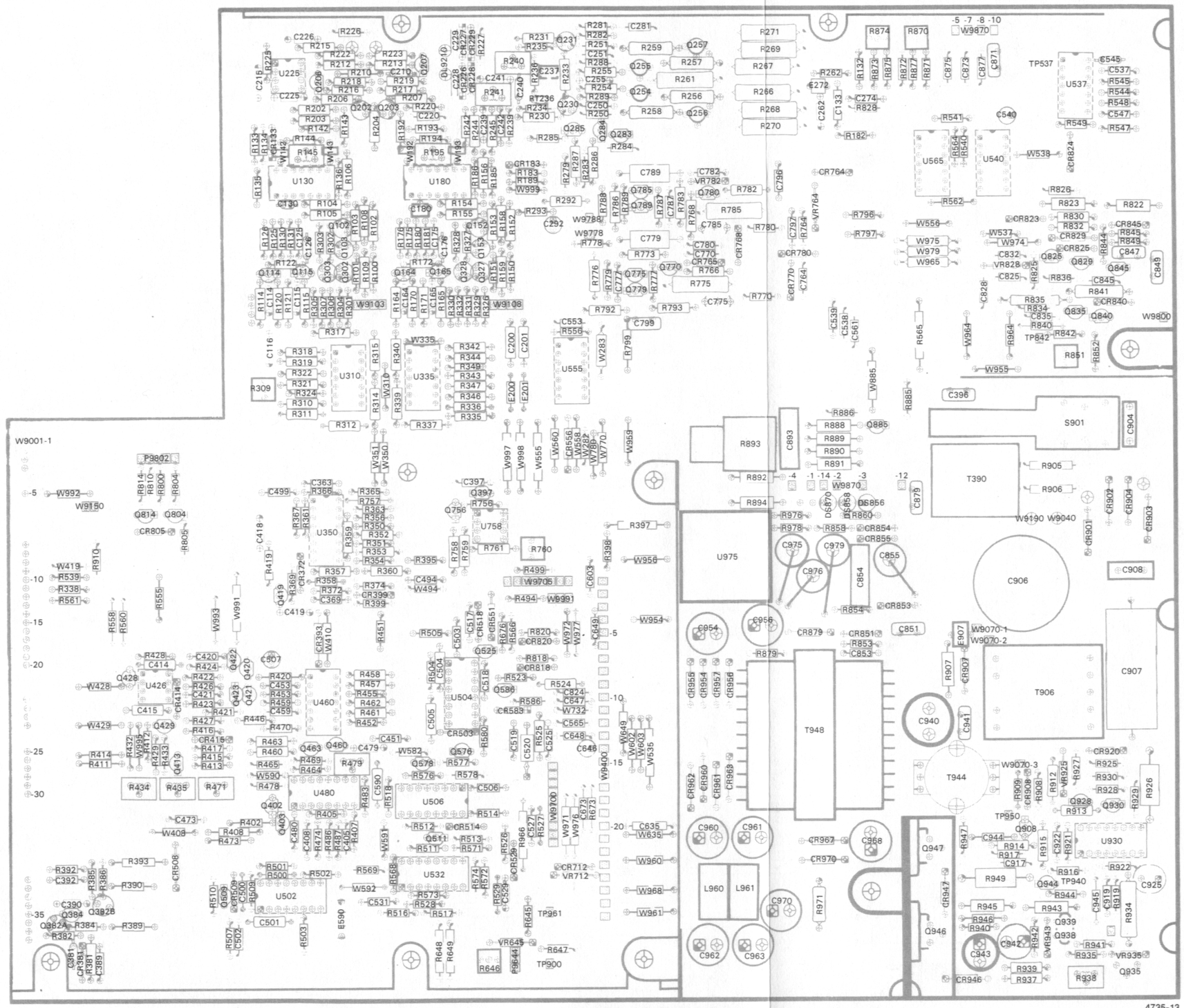
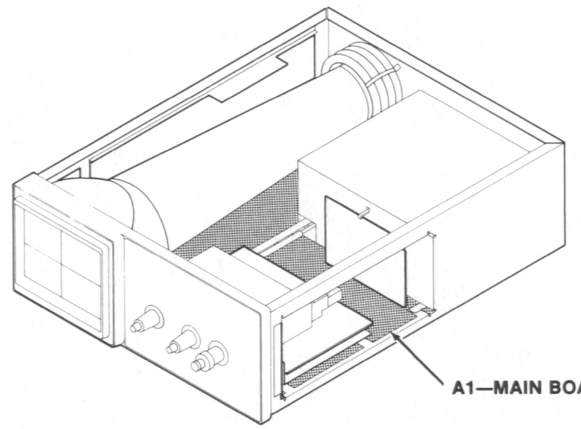


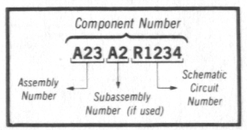
Figure 9-7. A1—Main board.



A1—MAIN BOARD

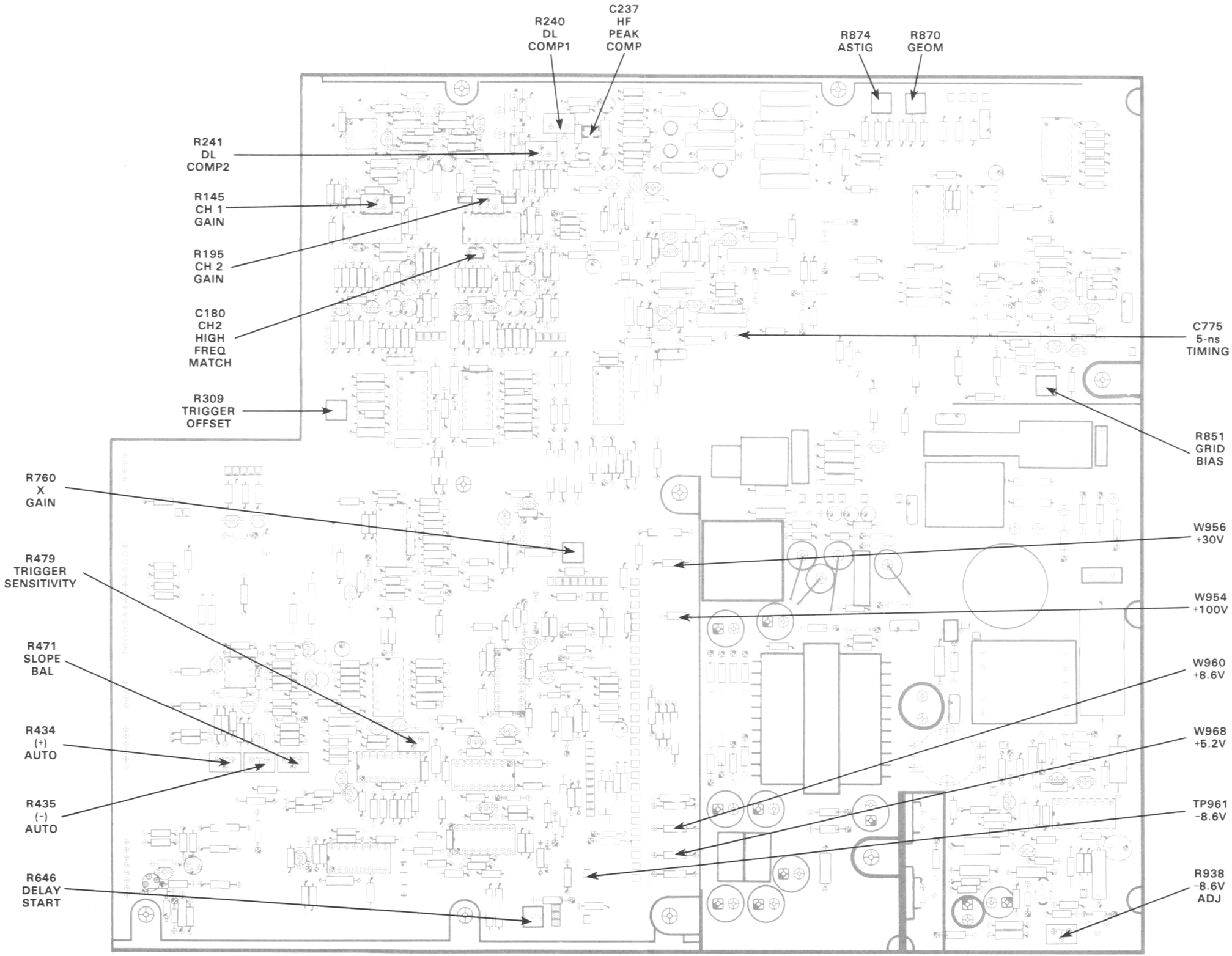
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



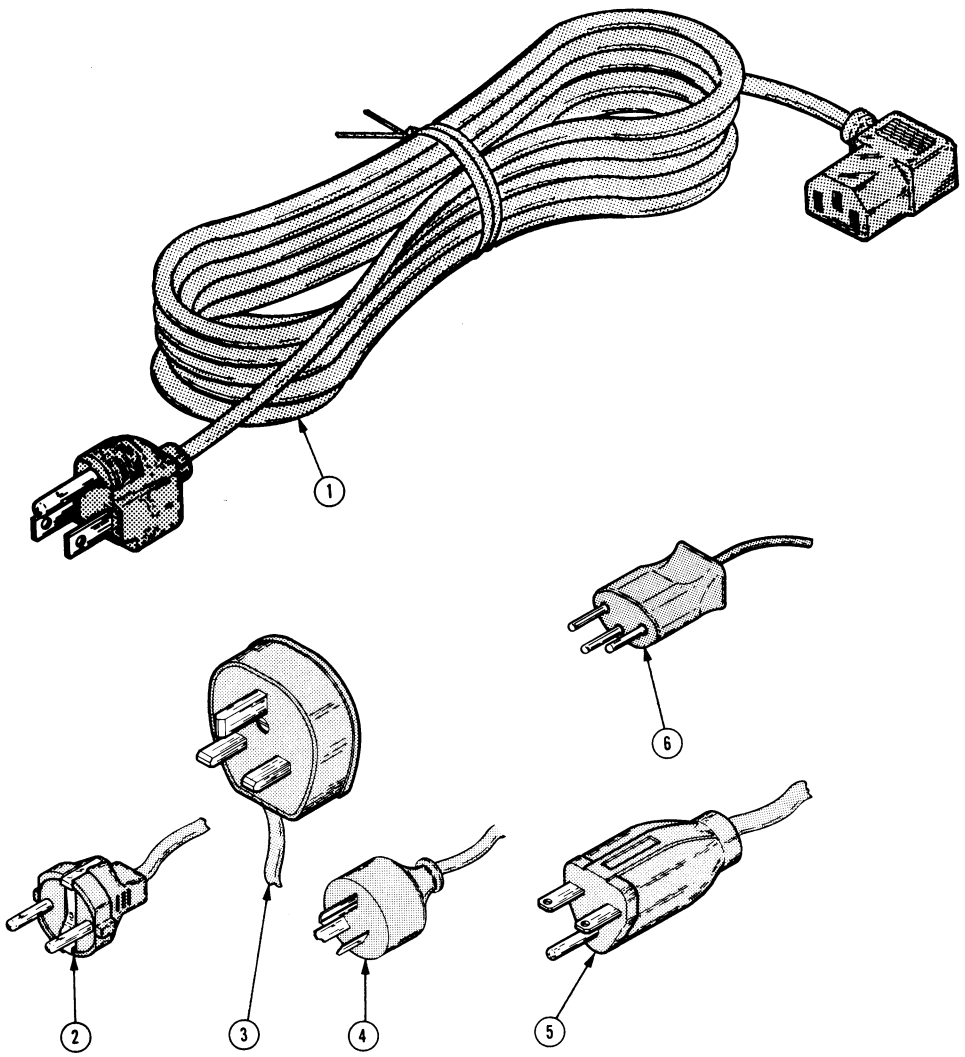
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

4735-13



4735-31

A1—MAIN BOARD ADJUSTMENT LOCATIONS


1
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MANUAL CHANGE INFORMATION

Date: 6-6-84 **Change Reference:** C1/0684

Product: 2215A SERVICE **Manual Part No.:** 070-4735-00

DESCRIPTION PG 46

EFFECTIVE ALL SERIAL NUMBERS

TEXT CHANGES

Page 5-19—5-20 Step 2.

Replace 2. Adjust Trigger Sensitivity (R479) with the following procedure.

2. Adjust Trigger Sensitivity (R479) and (R627)

a. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	0.1 V
AC-GND-DC (both)	AC
A and B SEC/DIV	10 μs

b. Connect the leveled sine-wave generator output via a 50-Ω cable and a 50-Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50-kHz, 2.2-division display.

d. Set the CH 1 VOLTS/DIV switch to 1 V.

e. ADJUST—A Trigger Sensitivity (R479) while rotating the A TRIGGER LEVEL control slowly so that the A Trigger is just able to be maintained.

f. Adjust the A TRIGGER LEVEL control for a stable display.

g. Set the HORIZONTAL MODE switch to B.

h. ADJUST—B Trigger Sensitivity (R627) while rotating the B TRIGGER LEVEL contol slowly so that the B Trigger is just able to be maintained.

i. Return the HORIZONTAL MODE switch to A.

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A5R627	311-1921-00	RES,VAR,NONWIR: 250 OHM,10%,0.5W