

Testing IC Voltage Regulators

IC regulators have come into common usage in low-voltage power supplies. The 178 can display the parameters of these devices when the Regulator test card is installed.

Fig. 11 shows the basic circuit configuration when this card is installed. The Sample and Hold Amplifier nullifies effects of DC output voltage on the Device Under Test. The output of the Feedback Amplifier is proportional to the AC changes at the output of the Device Under Test.

Just as for amplifier ICs, the 178 allows IC regulators

to be tested under conditions approximating those of the actual circuit. Some of the tests which can be made are measurement of output voltage, line regulation, load regulation, and measurement of input current.

Summary

The 577/177/178 Curve Tracer system joins many other TEKTRONIX instruments which help the engineer to better understand the discipline in which he works. This system expands component measurements and makes them easier for better product specification by the manufacturer, more effective circuit design by the engineer, and quicker instrument repair by the service technician.

ACKNOWLEDGMENTS

Jack Millay headed up the very able team which designed the 577 Curve Tracer Measurement System. Working on the electrical design were Jim Knapton, Bob Herb, Bob Verrinder, Om Agrawal, Dave Rule, and Gary Davis. Tom Saucy did the mechanical design while Darrell Barrett and Gil Stephens provided evaluation support. Lena McIntosh and Iona MacKay built the prototype instruments. And there were many others who helped in both large and small ways to make this project a success.

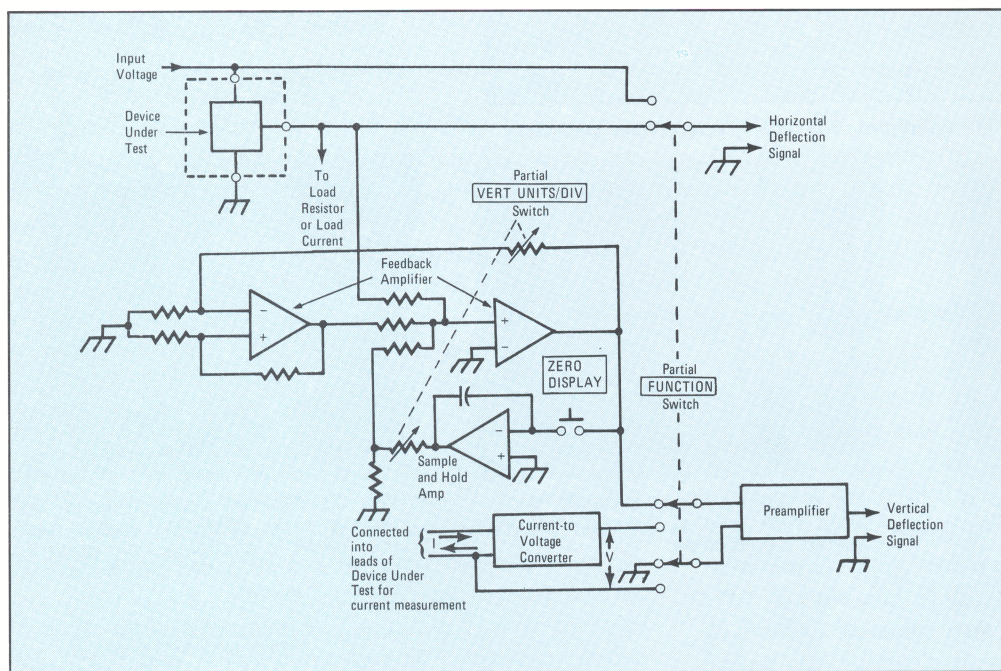
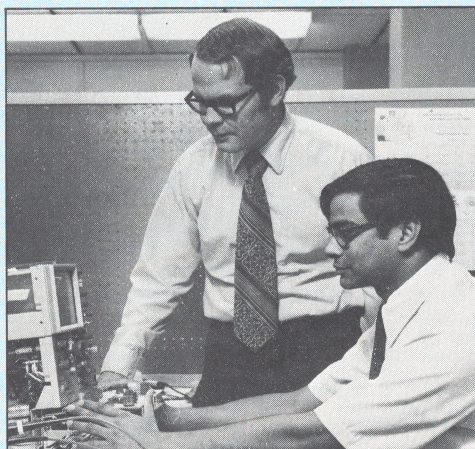


Fig. 11. Block diagram of the 178 configured for testing IC regulators.

OUR AUTHORS



Jack Millay

Jack attended Multnomah College before joining TEK in 1958. As manager of the Curve Tracer Engineering Group, he has been involved in most of the recent advancements in this area and has authored several previous articles for TEKSCOPE.

Jack is married and has two children. When not working with curve tracers, he enjoys flying, bee keeping, and antique cars.

Om Agrawal

Om is a native of India and received his Bachelors of Technology in Electrical Engineering at the Indian Institute of Technology, Kanpur, India. After coming to the U.S., he attended the Case Institute of Technology, receiving an M.S.E.E. He is presently attending the University of Portland where he plans to receive an M.B.A. degree in December.

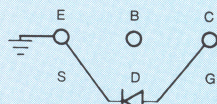
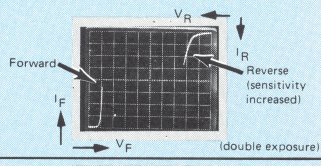
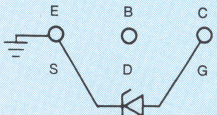
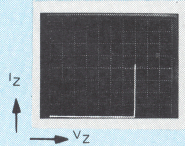
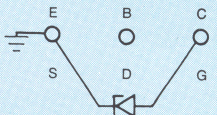
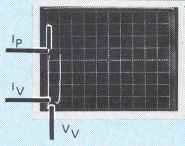
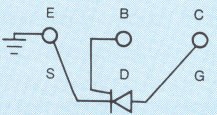
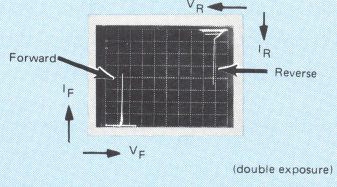
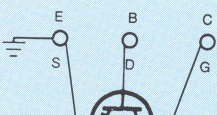
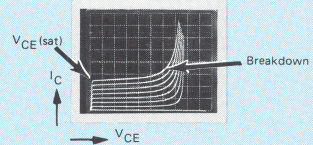
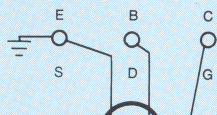
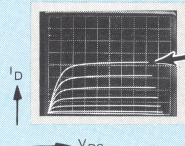
Since starting at TEK in 1970, Om has worked on the 172 as well as the current 577/177/178 project. When not working or studying, he enjoys swimming and roller skating.

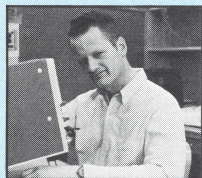
the enhancement region, pull out the STEP OFFSET knob and adjust up to 5 steps of opposing offset. Since the offset is uncalibrated, the zero bias (I_{DSS}) point must be marked in some manner.

Pinch off voltage V_p is measured by increasing the STEP AMPL and STEP controls until a specified pinch off current is reached. V_p is the step amplitude multiplied by the number of steps required to reach pinch off.

Summary

The 5CT1N and 7CT1N are designed to give a rapid check of device characteristics. Only a few of the checks which can be made have been discussed here. For more detailed information or for further tests, see either the Tektronix Measurement Concepts Book "Semiconductor Device Measurements" (P/N 062-1009-00) or the instruction manual for the particular plug-in.

5CT1N/7CT1N BASIC MEASUREMENT REFERENCE CHART			
DEVICE	CONTROL SETTINGS	CONNECTIONS	TYPICAL WAVEFORM
A. Signal & Power Diodes	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ NPN-PNP XSTR-FET	MIN Out (.5 V) Out (X1) 1 mA/DIV In ($\div 1$) Out (NPN) Out (XSTR)	 
B. Zener Diodes	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ NPN-PNP XSTR-FET	MIN As needed As needed 1 mA/DIV In ($\div 1$) Out (NPN) Out (XSTR)	 
C. Tunnel Diodes	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ NPN-PNP XSTR-FET	MIN Out (.5 V) Out (X1) 1 mA/DIV In ($\div 1$) Out (NPN) Out (XSTR)	 
D. SCR & SCS	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ STEP OFFSET STEP AMPL STEP NPN-PNP XSTR-FET	MIN Out (.5 V) Out (X1) 10 mA/DIV In ($\div 1$) In (off) 1 mA/step ccw Out (NPN) Out (XSTR)	 
E. NPN - PNP Transistors	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ STEP OFFSET STEP AMPL STEP NPN-PNP XSTR-FET	MIN In (2 V) Out (X1) 1 mA/DIV In ($\div 1$) In (off) 5 μ A/step ccw Match Transistor Out (XSTR)	 
F. Field Effect Transistors	COLLECTOR/DRAIN VOLTS .5 V - 2 V X10 VERTICAL $\div 1000$ STEP OFFSET STEP AMPL STEP NCh(+)-PCh(-) XSTR-FET	MIN In (2 V) Out (X1) .5 mA/DIV In ($\div 1$) In (off) .2 V/step ccw Match FET In (FET)	 



Matt Zimmerman—Matt began his electronics training while in the U.S. Navy and continued his studies to receive an Associate Degree in Electronics from Long Beach City College. In his six years at TEK, Matt has worked in the Standards Lab, CRT Support, and now as Design Technician in the 5100-Series group. Among the products he has worked on here are the 5CT1N/7CT1N, 5100 Series, and TM 500 Series.

Matt is married and has two children. In his spare time, he is building a new house for his family.

FEATURES	DIFFERENTIAL	ADDED MODE	COMMENTS
Typical CMRR	Typically between 10,000:1 to 100,000:1 from DC to 100 kHz	100:1 or greater at 50 kHz (422 Spec)	Using the "ADDED" mode, CMR can be optimized by connecting Channels 1 & 2 inputs to a common source (calibrator) and adjusting Channel 1 or 2 GAIN for minimum CM display.
Probes CMRR Compensatable or matched for CMRR	YES	NO	
Balanced Input Circuits	YES	NO	With the "ADDED" mode, input RC input TC may vary within $\pm 2\%$ between channels.
Input Amplifiers Phase Corrected	YES	NO	
High Sensitivity	YES	NO	Typical for "ADDED" 5 mV/div (453A) Typical for differential 10 μ V/div (7A22)
High Input Impedance	YES See Comments	NO Nominal 1 meg-ohm input impedance	This feature is either switchable (W unit) or by strap removal, (7A22, 5A22N)

Fig. 2. Table showing the relative merits of a true differential amplifier and one using the "ADDED" mode technique.

The Differential Comparator

You will recall in Part 1 of this series we stated that the differential amplifier appears in two basic forms: namely, the paraphase type and the push-pull. The only difference between the two is that the paraphase has one input referenced to a fixed potential—this is the basic form of the differential comparator. To make it useful, the fixed potential is replaced by a calibrated variable DC supply which is called the comparison voltage (V_c).

Fig. 3 shows a functional block diagram of a typical differential comparator system. Notice that we can operate this unit as a conventional differential amplifier by simply switching to the A-B mode with the DISPLAY switch.

Let's see how we go about making a differential comparator measurement. First, we establish a reference position on our display by grounding both inputs. Then, selecting the appropriate input (positive voltage source to the + INPUT, negative voltage source to the - INPUT), we switch the other input to the comparison voltage (V_c). Next, the comparison voltage is adjusted until the trace "slides back" to the reference position. What have we accomplished? Using the "difference" principle we have introduced a "common-mode" condition in the form of the comparison voltage; that is, the comparison input voltage now equals the signal input. We see that we now have the ability to measure any potential whether it be DC, complex in nature, or a combination of both—such as a complex wave superimposed on a DC potential. Thus, we have an extremely versatile measuring tool. Notice, however, it does not have the mechanism to reject any interfering signal.

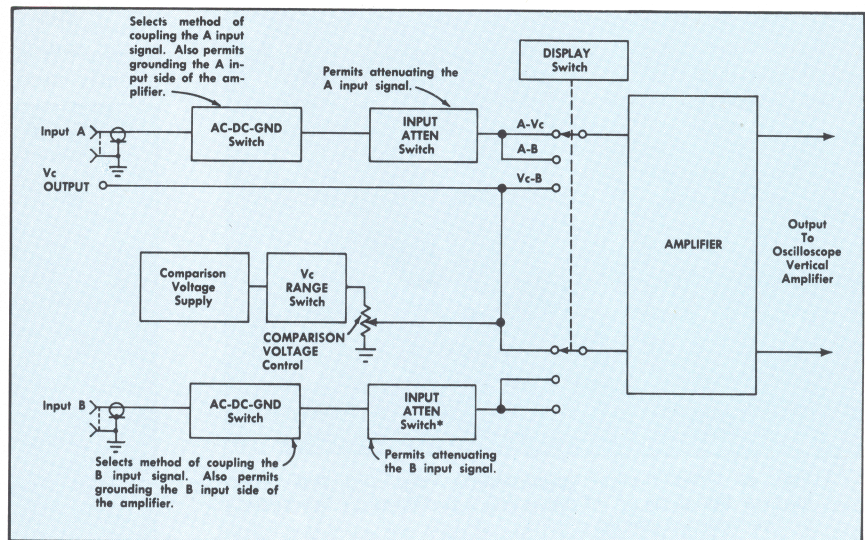


Fig. 3. A block diagram of a typical differential comparator. Notice when the DISPLAY mode switch is in the A-B position the unit becomes a conventional amplifier.

From the practical point of view, we must recognize some limitation when making comparator measurements. In order to measure a large potential or a waveform which is superimposed on a large potential, it may be necessary to attenuate the input signal to within acceptable limits to prevent damage to the input circuits. The first thing we must recognize is that the probes and/or attenuators, plus the comparison voltage circuits, will introduce an error by the amount they deviate from their true value. Simply stated, a resistance divider with a tolerance of $\pm 0.1\%$ will introduce that same error to our final reading. You must be aware of these limitations when making an absolute measurement with a differential comparator. These errors may differ from instrument to instrument so it is advisable to check your instrument manual for these details.

DC OFFSET

When making a differential measurement with a con-